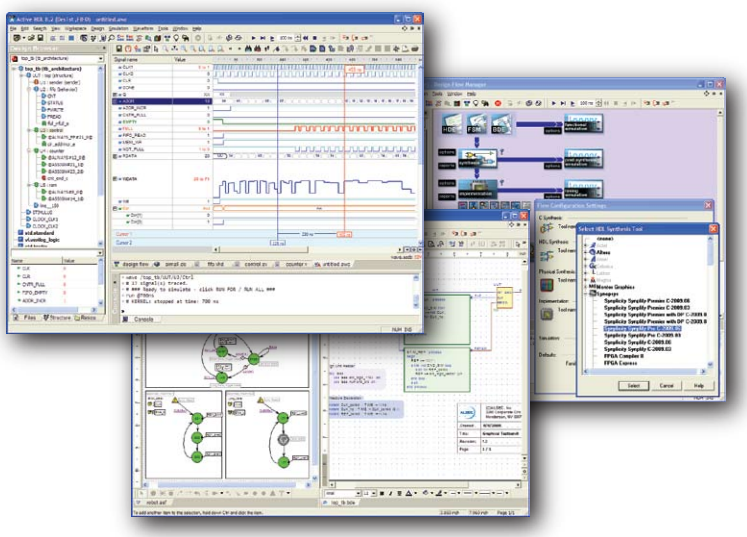
# FPGA Design and Simulation Made Easy

## Active-HDL™

Active-HDL is an integrated FPGA Design and Simulation solution, with design entry, a high-performance mixed-language simulator and an easy-to-use, multi-vendor FPGA flow manager that controls Simulation, Synthesis and Implementation for industry leading FPGA devices, from Actel™, Altera®, Lattice®, Quicklogic® and Xilinx®. Active-HDL has interfaces to over 80 leading EDA tools, making it the most powerful environment.



## Top Features

- Graphical Design Entry
- High Performance Mixed-Language RTL Simulator
- IEEE VHDL, Verilog®, SystemVerilog (Design), SystemC
- Advanced Debugging & Code Coverage
- IP Encryption based on IEEE Standards
- Assertion-Based Verification (ABV)
- DSP Co-simulation with MATLAB®/Simulink®
- PCB Design Interface
- HTML and PDF Design Documentation
- Windows® 7/Vista/XP/2003 32/64 bit support

## High Performance, Mixed-Language Simulation

Active-HDL includes a high performance, common-kernel, mixed-language simulator supporting batch mode simulation, VCD, a performance profiler, memory viewer, encrypted IP and FPGA vendor libraries. Drive your system-level simulation model using complex testbenches or create quick and flexible stimulator farms to rapidly test design modules and system-level designs.

## Graphical Design Entry

Draw any finite state machine diagram and let Active-HDL generate your synthesizable RTL code. Connect all design modules at the top-level and automatically generate output structural HDL using the built-in block diagram editor. If needed, convert HDL to graphics with Code2Graphics™ utility. Active-HDL can also import, re-target, enhance, simulate and debug your legacy designs.

## Debugging and Code Coverage

Active-HDL includes state-of-the-art debugging with an Accelerated Waveform, with cross-probing to HDL source code, breakpoint management, testbench and stimulus generation. A powerful HDL code coverage analyzer provides 100% test coverage of all statements, lines, signals, toggle, branch, path and logical expressions in the design.

## STANDARDS

accellera
EDA CONSORTIUM
IEEE
SYSTEMC
SystemVerilog

## SILICON

Actel POWER MATTERS
achronix SEMICONDUCTOR CORPORATION
ALTERA
tabula
Lattice Semiconductor Corporation
QuickLogic
XILINX

## INTERFACES

ARM
Altium
cadence
MAGMA
The MathWorks
Mentor Graphics
SYNOPSYS
ZUKEN

PRO HDL ALINT HES MIL/AERO

# FEATURES / PRODUCT CONFIGURATIONS

| Design Entry | DM | Designer Edition | PE | EE |
|---|---|---|---|---|
| HDL, Text, Block Diagram and State Machine Editor | • | • | • | • |
| Language Assistant with Templates and Auto-Complete | • | • | • | • |
| Macro, Tcl/Tk, Perl script Support | • | • | • | • |
| Pre-compiled FPGA Vendor Libraries | • | • | • | • |
| Code2Graphics™ Converter | • | | • | • |
| Legacy Schematic Design Import and Symbol Import/Export | • | | • | • |
| **Supported Languages** | | | | |
| Single or Mixed Language Design Support | Mixed Only | Mixed Only | • | • |
| VHDL IEEE 1076 (1987, 1993, 2002 and 2008) | • | • | • | • |
| Verilog® HDL IEEE 1364 (1995, 2001 and 2005) | • | • | • | • |
| SystemVerilog IEEE 1800™-2005 (Design) | • | • | • | • |
| SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0 | | | Option | • |
| **Code Generation Tools** | | | | |
| Testbench Generation from Waveforms | | | • | • |
| Testbench Generation from State Diagram | | | • | • |
| **Project Management** | | | | |
| Design Flow Manager for All FPGA Vendors | • | • | • | • |
| Revision Control Interface | • | • | • | • |
| **Simulation/Verification** | | | | |
| Simulation Performance (Baseline 2X Faster than FPGA Vendor Supplied Simulator) | | Baseline | 3X Baseline | Up To 6X Baseline |
| Simulation Model Protection/Library Encryption | | • | • | • |
| VHDL/Verilog IEEE Compatible Encryption | | • | • | • |
| Value Change Dump (VCD and Extended VCD) Support | | • | • | • |
| Verilog Programming Language Interface(PLI/VPI) | | • | • | • |
| VHDL Programming Language Interface (VHPI) | | | • | • |
| Batch Mode Simulation/Regression (VSimSA) | | | • | • |
| Xilinx SecureIP Support | | • | Option | • |
| Profiler (Performance Metrics) | | | Option | • |
| Verilog HDL Simulation Optimization | | | | • |
| VHDL Simulation Optimization | | | | • |
| **HDL Debug and Analysis** | | | | |
| Interactive Code Execution Tracing | | • | • | • |
| Advanced Breakpoint Management | | • | • | • |
| Memory Viewer | | • | • | • |
| Waveform Viewer + Editor | | Viewer Only | • | • |
| Waveform Stimulator | | • | • | • |
| Waveform Compare | | | • | • |
| Post-Simulation Debug | | | • | • |
| C++ Debugger | | | • | • |
| Signal Agent (VHDL and Mixed Only) | | | • | • |
| X-Trace | | | Option | • |
| Advanced Dataflow | | | Option | • |
| **Coverage Tools** | | | | |
| Code, Statement, Branch, Expression, Condition and Toggle Coverage | | | Option | • |
| Functional Coverage in Assertions/Code Coverage | | | Option | Option |
| Path Coverage (VHDL Only) | | | | • |
| **Design Rule Checking** | | | | |
| ALINT™ with Aldec Basic Rule Library | | | Option | • |
| DO-254 VHDL or Verilog Rule Library | | | Option | Option |
| STARC® VHDL or Verilog Rule Library | | | Option | Option |
| **External Simulation Interfaces** | | | | |
| Synopsys® SmartModels, SWIFT interface and LMTV | | | Option | • |
| **Co-Simulation** | | | | |
| Simulink® Co-Simulation | | | • | • |
| MATLAB® Co-Simulation | | | Option | • |
| **Assertions Bundle** | | | | |
| PSL IEEE 1850, SystemVerilog IEEE 1800™, OpenVera Assertions | | | Option | Option |
| **Documentation** | | | | |
| Export to PDF/HTML/Bitmap Graphics | • | | • | • |
| Advanced Export to PDF (Vector Graphics) | Option | | • | • |
| **Specialty Solutions** | | | | |
| PCB Interface | | | • | • |
| SFM (Server Farm Manager) | | | Option | Option |
| **Supported Platforms** | | | | |
| Windows® 7/Vista/XP/2003 32/64 bit | • | • | • | • |


**Headquarters**
2260 Corporate Circle
Henderson, NV 89074
**Phone:** 702.990.4400
**Fax:** 702.990.4414
**E-mail:** sales@aldec.com

**Europe**
70 rue Cortambert
75116 Paris, France
**Phone:** 33.6.80.32.60.56
**Fax:** 33.1.46.34.85.91
**Email:** sales-eu@aldec.com

**Japan**
Shinjyuku Estate Bldg. 9F
1-34-15, Shinjyuku, Shinjyuku-ku
Tokyo 160-0022, Japan
**Phone:** 81.3.5312.1791
**Fax:** 81.3.5312.1795
**Email:** info@aldec.co.jp

**China**
Suite 2004, BaoAn Building
#800 DongFang Road
PuDong District
Shanghai City 200122, P.R. China
**Phone:** 86.21.6875.20.30
**Fax:** 86.21.6875.0083
**Email:** info@aldec.com.cn

**India**
P-186, Sector 10
Jiwan Bima Nagar
Bangalore
India-560075
**Phone:** 91.80.4150.6434
**Email:** sales-sa@aldec.com


ALDEC
**www.aldec.com**